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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/586,821	07/19/2006	Tetsuji Omura	YKI-0208	5381
23413 7590 06/30/2008 CANTOR COLBURN, LLP 20 Church Street 22nd Floor Hartford, CT 06103				
EXAMINER RALEIGH, DONALD L				
ART UNIT		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/586,821

Applicant(s)

OMURA ET AL.

Examiner

DONALD L. RALEIGH

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 July 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SF/ICE)
Paper No(s)/Mail Date 07/19/2006, 09/06/2006, 04/05/2007, 10/05/2007
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claims 1-12 are pending in the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3, and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto et al (JP Pub. No. 2001-189191), Takaoka et al (JP 01-234339) , Hsiao et al (US PG Pub. No. 2004/0241920) , Dunham et al (US PG Pub. No. 2003/0141804) and Jaeger (US Patent No. 5,867,149).

Regarding Claim 1, Matsumoto discloses, at least in Figures (Drawings) 1-8a display panel (abstract) manufacturing method, the display panel including an element substrate (1) with electroluminescent elements (abstract (EL)) formed thereon and a sealing substrate (17Figure 3) bonded to the element substrate (1) at a peripheral panel bonding part (see drawing 4 and Paragraph [0017]), thereof for sealing a space

over the element substrate (1), comprising the steps of: forming a frame-shaped groove (2)(Figure 1) on the panel bonding part of the sealing substrate (1) ,

Matsumoto fails to disclose forming a frame-shaped glass paste layer by introducing a paste including a low melting point glass powder and a solvent into the groove, conducting a thermal processing by volatilizing the solvent contained in the glass paste layer to provide a low melting point glass frame, forming a low heat resistant layer on the surface of the sealing substrate, the low heat resistant layer made of a material having a heat resistant temperature lower than the temperature of the thermal processing, and with the element substrate arranged to face the sealing substrate at a predetermined distance, sealing a space between the element substrate and the sealing substrate by directing a laser beam to the low melting point glass frame to heat and melt the low melting point glass, so that the low melting point glass is raised towards the element and the two substrates are welded together along the peripheries thereof by the raised glass.

Takaoka teaches (see abstract) using low melting point glass powder with a solvent to form a paste; heating the glass paste (which would volatilize the solvent) and heating until the glass melts. Takaoka acknowledges the use of the disclosed sealing material in IC packaging, the sealing being free of pin holes and having excellent air tightness.

Accordingly, it would have been obvious to one of ordinary skill in the art, at the time of the invention to use the sealing material and testing process disclosed by

Takaoka in the method of Matsumoto in order to provide a sealant free of pin holes and having excellent air tightness.

Jaeger teaches in Column 10, lines 37-39 using a laser beam to melt low melting point glass so that the low melting point glass is raised towards the element and the two substrates are welded together along the peripheries thereof by the raised glass.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the use of a laser beam to melt the low melting point glass, as taught by Jaeger, into the device of Matsumoto, as modified by Takaoka, in order to concentrate the heating of the substrate to the periphery, thereby protecting the interior elements from heat damage.

Hsiao teaches In Paragraph [0004], lines 6-7 placing a color filter layer on the top glass substrate. Hsiao also teaches in Paragraph [0005], lines 17-18 that the color filter cannot withstand temperatures exceeding 300 degrees C. . Hsiao teaches In Paragraph [0004], lines 6-7 placing the color filter layer on the top glass substrate for allowing transmission of predetermined light wavelengths and enhance color purity.

Dunham teaches in Paragraph [0044], lines 6-10, that to melt the frit (thermal melting point frame) requires temperatures above 300 C.(higher than the heat resistant temperature of the color filter layer).

It would have been obvious to one of ordinary skill in the art, at the time of the invention to incorporate the low heat resistant layer (color filter) as taught by Hsiao into the device of Matsumoto, as modified by Takaoka and Jaeger, for allowing transmission of predetermined light wavelengths and enhance color purity.

Regarding Claim 3, Matsumoto, as modified by Takaoka, Jaeger and Dunham fails to exemplify the display panel wherein the low heat resistant layer formed in the step of forming the low heat resistant layer is at least one of a color filter, a resinous black matrix, a polarizer, and a phase plate.

Hsiao teaches, in Paragraph [0004], lines 6-7, a color filter layer on the top glass substrate. Hsiao also teaches in Paragraph [0005], lines 17-18 that the color filter cannot withstand temperatures exceeding 300° C (low heat resistant). Hsiao teaches In Paragraph [0004], lines 6-7 placing a color filter layer on the top glass substrate for allowing transmission of predetermined light wavelengths and enhance color purity.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the low resistant color filter layer, as taught by Hsiao, into the display device of Matsumoto, as modified by Takaoka, Jaeger and Dunham, on the top glass substrate for allowing transmission of predetermined light wavelengths and enhance color purity.

Regarding Claim 6, Matsumoto discloses in Figure 4 (Drawing 4) wherein the groove formed in the groove forming step has a tapered cross section, with the width of the groove gradually narrowing from the surface of the sealing substrate towards the bottom of the groove. (The groove of Figure 4 has a rounded bottom and therefore, is narrower at the bottom than the top).

Regarding Claim 7, Matsumoto discloses in Figure 4 (Drawing 4) wherein the bottom of the groove has a smoothly curved cross section. The groove shown in Figure 4 has a rounded bottom.

Claims 8, and 10-11 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Matsumoto et al (JP Pub. No. 2001-189191) in view of Beteille et al (US Patent No. 7,033,655)

Regarding Claim 8, Matsumoto discloses, at least in Figures (Drawings) 1-8, a display panel (abstract) comprising an element substrate (1)) with electroluminescent elements (abstract (EL)) formed thereon and a sealing substrate (17)(drawing 3 and Paragraph [0017]) which is bonded to the element substrate (1) at a peripheral panel bonding part (see drawing 4)(Paragraph [0017]) thereof for sealing a space over the element substrate (1), wherein the element substrate (1) and the sealing substrate (17) are sealed and welded together along the peripheries .

Matsumoto fails to disclose that the sealing of the substrates is done with a low melting point glass, and a portion of the low melting point glass is introduced into a frame shaped groove formed in the sealing substrate

Beteille teaches in an electroluminescent device (Column 1, line 45), a low melting point glass and a portion of the low melting point glass is introduced into a frame shaped groove. Figure 1 of Beteille shows a seal (5) in a peripheral groove (Column 9, lines 33-35) and that this seal can include a frame of low melting point glass

(Column 6, lines 50-52).Beteille provides this frame to reinforce the glazing (improve the mechanical strength) of the seal (Column 5, lines 19-21).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to incorporate the sealing structure, as taught by Beteille, into the display device of Matsumoto, to reinforce the glazing and improve the mechanical strength of the seal.

Regarding Claim 10,Matsumoto discloses in Figure 4 (Drawing 4) wherein the groove has a tapered cross section, with the width gradually narrowing from the surface of the sealing substrate towards the bottom of the groove. The groove shown in Figure 4 has a rounded bottom and thus is wider at the top.

Regarding Claim 11,Matsumoto discloses in Figure 4 (Drawing 4) wherein the bottom of the groove has a smoothly curved cross section. The groove shown in Figure 4 has a rounded bottom.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Takaoka (339), Jaeger, Hsiao (920) , Dunham (804) and further in view of Shimizu et al (US PG Pub. No. 2002/0030437) and Sagara (US Patent No. 5,997,377).

Regarding Claim 2, Matsumoto, as modified by Takaoka, Jaeger, Hsiao , and Dunham fails to exemplify the display panel wherein the step of forming the glass paste layer includes introducing the glass paste into the frame-shaped groove in an amount

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exceeding the volume of the groove, and the method further includes, after volatilizing the solvent in the thermal processing, flattening the surface of the bonding part of the sealing substrate by removing a part of the low melting point glass frame extending over the surface of the sealing substrate.

Shimizu teaches in Paragraph [0097] introducing the glass paste (line 1) into the frame shaped groove (lines 5-8 (grooves of the frame)), volatilizing the solvent (lines 3-4, resin dispersion medium) in the thermal processing (line 19, the solvent is volatilized at 450° C). Shimizu fails to teach flattening the surface of the bonding part of the sealing substrate by removing a part of the low melting point glass frame extending over the surface of the sealing substrate.

Sagara teaches wherein in the flattening step (Column 11, line 58 (flatness)), the low melting point glass frame (line 57) extending over the surface of the sealing substrate (15)(line 57) is removed by polishing (line 58) in order to improve flatness.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the polishing method, as taught by Sagara into the method of Jaeger, as modified by Takaoka, Jaeger, Hsiao and Dunham, in order to improve flatness.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Takaoka (339), Jaeger (149), Hsiao (920) and Dunham (804) and further in view of Sagara (US Patent No. 5,997,377).

Regarding Claim 4, Matsumoto, as modified by Takaoka, Jaeger, Hsiao and Dunham, fails to exemplify the display panel manufacturing method wherein in the

flattening step, the low melting point glass frame extending over the surface of the sealing substrate is removed by polishing.

Sagara teaches wherein in the flattening step (Column 11, line 58 (flatness)), the low melting point glass frame (line 57) extending over the surface of the sealing substrate (15)(line 57) is removed by polishing (line 58) in order to improve flatness.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the polishing method, as taught by Sagara into the method of Matsumoto, as modified by Takaoka, Jaeger, Hsiao and Dunham, in order to improve flatness.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Takaoka (339), Jaeger (149), Hsiao (920) and Dunham (804) and further in view of Kawashima (US PG Pub. No. 2005/0029513).

Regarding Claim 5, Matsumoto, as modified by Takaoka, Jaeger, Hsiao and Dunham, discloses the low melting point glass frame but fails to exemplify the display panel wherein in the flattening step, the low melting point glass frame extending over the surface of the sealing surface is removed to make the surface irregularities of the bonding part of the sealing substrate to not more than 1/10 of the film thickness of the low heat resistant layer which is formed subsequent to the flattening step.

Kawashima teaches wherein in the flattening step, the low melting point glass frame extending over the surface of the sealing substrate (Paragraph [0215]) is removed to make the surface irregularities of the bonding part of the sealing substrate

to not more than 1/10 of the film thickness of the low heat resistant layer which is formed subsequent to the flattening step. (Paragraph [0451] teaches that the low heat resistant layer (the color filter) is 6 microns in thickness. Paragraph [0524], Claim 17 teaches that the maximum variation in the roughness of the substrate is 60 nm (which includes the bonding area). In such case, the irregularities of the surface are 1/1000 th the film thickness of the low heat resistant layer. Furthermore, to achieve this, the surface irregularities of the bonding part of the sealing substrate would have to be removed, i.e. a flattening step would have to be taken. Kawashima does this in order to provide a gas barrier substrate having a high gas barrier property without a ruggedness, a pin hole or the like in the gas barrier layer. (abstract, lines 1-3).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the flattening method, as taught by Kawashima, into the display panel of Matsumoto, as modified by Takaoka, Jaeger, Hsiao and Dunham, in order to provide a gas barrier substrate having a high gas barrier property without a ruggedness, a pin hole or the like in the gas barrier layer.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Beteille et al (US Patent No. 7,033,655) and further in view of Hsiao et al (US PG Pub. No. 2004/0241920).

Regarding Claim 9, Matsumoto, as modified by Beteille, fails to exemplify the display panel wherein at least one of a color filter, a resinous black matrix, a polarizer,

and a phase plate is provided on the surface of the sealing substrate facing the element substrate.

Hsiao teaches In Paragraph [0004], lines 6-7 places a color filter layer on the top glass substrate for allowing transmission of predetermined light wavelengths and enhance color purity.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the color filter, as taught by Hsiao into the display panel of Matsumoto, as modified by Beteille, for allowing transmission of predetermined light wavelengths and enhance color purity.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto in view of Beteille (655), and further in view of Sun et al (US PG Pub. No. 2004/0160184).

Regarding Claim 12, Matsumoto, as modified by Beteille, fails to disclose wherein in the direction of the width of the groove, the thickness of the low melting point glass used for bonding the element substrate to the sealing substrate is less than the width of the groove.

Sun teaches wherein in the direction of the width of the groove (Page 4, right column line 1, 0.3mm to 1.5mm) is the width of the seal and figures 3-7 show the seal (3) confined to the groove. Page 4, right column line 2 states that the thickness of the sealant is 0.05mm to 0.2mm, considerably less than the width of the groove. Page 4, left column, lines 3-4 states that the seal is a low melting point glass. Sun does this to

provide an improved display panel (PDP) with narrower sealing parts.(Paragraph [0007], lines 1-4)

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to incorporate the bonding structure as taught by Sun into the method of Matsumoto, as modified by Beteille, in order to provide an improved display panel with narrower sealing parts.

Conclusion

Examiner's note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DONALD L. RALEIGH whose telephone number is (571)270-3407. The examiner can normally be reached on Monday-Friday 7:30AM to 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel can be reached on 571-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Donald L Raleigh/
Examiner, Art Unit 2879

/Mariceli Santiago/
Primary Examiner, Art Unit 2879